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New Three-Phase AC-DC Rectifiers with Reduced Numbers of Switches

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Keywords: ac-dc rectifiers; four-switch three-phase (FSTP) rectifier.

Abstract

DC-AC rectifiers with reduced numbers of switches, in order to reduce cost, weight, volume and switching losses (especially for low-power applications), have been presented and discussed in the literature. These converters are less exposed to semiconductor switch damage and exhibit lower common-mode currents. However, they have several disadvantages when compared with conventional six-switch three-phase (SSTP) rectifiers, such as dc-link capacitor voltage fluctuation, reduced input ac supply utilisation factor, and unbalanced three-phase input currents. This paper proposes new designs for four-switch three-phase (FSTP) and two-switch single-phase rectifiers (TSSP). This paper explains the normal operation, and proposes beneficial comparisons and performance evaluation, of the proposed rectifiers. In addition, proper control design for the proposed converters is presented with sliding mode control (SMC).

1 Introduction

Presently, there is an international trend toward the reduction of CO_2 production worldwide [1]. Accordingly, the research and development of modern power systems and micro-grids have become more important and significant. Several converter topologies have been proposed and studied in order to enhance their operation, reduce total cost, and improve the efficiency of power systems.

Recently, many researches have considered three-phase Voltage Source Rectifiers (VSRs) with six semiconductor active switches [2]-[4]. and therefore, the literature for these topologies and their control strategies became mature.

However in several low-power applications, converter topologies with lower switch count may be demanded in order to reduce cost and size, and to increase system efficiency. In [5], the first three-phase two-level VSR with only four switches is presented, see Fig.1. In this four-switch three-phase (FSTP) rectifier, two of the input three-phase currents are connected to the two legs of the rectifier while the third phase is connected to the midpoint of the split capacitors across the dc output side. Operation, control design, and performance of FSTP rectifiers have been discussed extensively in the literature [6]-[9].

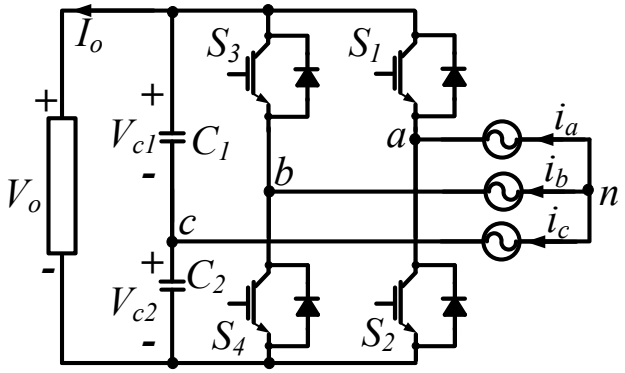


Fig.1. Conventional four-switch three-phase rectifier (FSTP).

The FSTP rectifier has several of the advantages of the conventional VSI, such as reduced total cost and lower power loss: hence, better efficiency can be obtained. In addition, the required numbers of gate drives circuits, measurement boards, and real-time calculations are less in the FSTP rectifier [3].

Moreover, the maximum common-mode current and voltage in FSTP rectifiers are reduced by 33% [3, 4]. The FSTP rectifier has lower probability of switch damage as the interaction between the active switches is less. The dc link voltage is doubled in comparison with the six-switch rectifier.

The main disadvantage of the FSTP rectifier is that dc current components may appear in the input ac current because the third input phase is connected directly to the dc output side. These dc current components are hazardous and a proper control effort should be conducted in order to suppress them. IEEE 1574 standards restrict the dc current components to <0.5% of the rated RMS current whilst IEC 61727 standards limit them to <1%.

In addition, fluctuation of the dc-link capacitor voltage at the fundamental frequency results in fluctuations of the FSTP rectifier input currents. The problem of dc-link voltage oscillation necessitates modified pulse-width modulated (PWM) signals to control and create the desired output voltage during the switching period [10]. Practically, the dc-link split capacitors may not have exactly equal capacitance values. Consequently, a control effort should be implemented in order to balance the capacitors voltages [10]. Also, the FSTP rectifier requires higher switching frequency in order to eliminate third-order harmonics from the input ac currents.

From the thirty-three possible two-switch two-diode bidirectional power electronic converters, there are four converters that can provide output voltage with positive and negative polarities. These converters are shown in Fig. 2 as

two voltage buck and two voltage boost converters. Based on these converters, new three-phase rectifiers with four switches can be generated. Unlike other FSTP rectifiers, the proposed converters do not have direct connection between the ac phases and the dc side voltage. Consequently, the problem of dc current generation in the ac grid does not exist. Moreover, because they do not require direct connection between the ac and dc sides, the proposed converters can operate as ac-dc rectifiers and dc-ac inverters. In ac-dc rectification mode, the proposed rectifiers double the maximum output dc voltage in comparison with the conventional FSTP rectifier.

Unfortunately, the proposed converters are time-variant systems, where the overall transfer function describing the relation between the input and output voltages and currents depends upon the switching periods of the switches. This results in a complex stable design because the converter poles and zeros travel through a long trajectory. Moreover, the time-varying transfer function leads to output voltage and current distortion [11, 12]. Converter stability and reliability decrease with increasing passive element values. However, reducing the inductor and capacitor values results in larger high-frequency ripple current and voltage components, and hence increases the total harmonic distortion (THD) of the input current and voltage. On the other hand, increasing the passive element values increases the stored energy inside the inverter, producing a third-order harmonic component and its multiples in the input dc current.

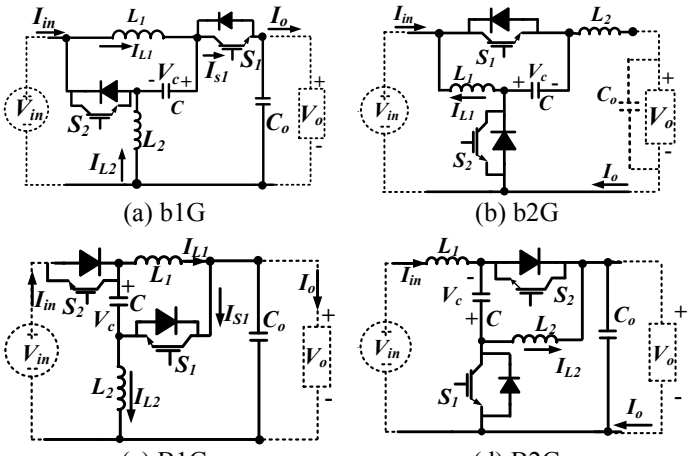


Fig. 2. DC-DC converters with bidirectional output voltages: (a) and (b) voltage-buck converters, (c) and (d) voltage-boost converters.

This paper presents new rectifier topologies with reduced numbers of switches based on the abovementioned bidirectional dc-dc converters. In addition, proper control design for the proposed converters is presented with sliding mode control techniques (SMC). Practical results substantiate the design flexibility of the proposed topologies when controlled by a TMSF280335 DSP.

2 DC/DC Converters with Positive and Negative Output Voltage

The four two-switch two-diode dc-dc converters with positive and negative output voltages are shown in Fig. 2. Two of these converters are voltage buck converters (b1G and b2G) whilst the other two are voltage boost converters (B1G and B2G). The relationship between the output and input voltages, V_o and V_{in} respectively, is defined by (1), where M is the voltage conversion ratio and D is the duty ratio of switch S_1.

$$M(D) = V_o / V_{in} \tag{1}$$

The voltage conversion ratios of the converters can be expressed as (2) and (3).

$$M(D) = \frac{2D-1}{D} \quad for \ \ b1G \ \ and \ \ b2G \tag{2}$$

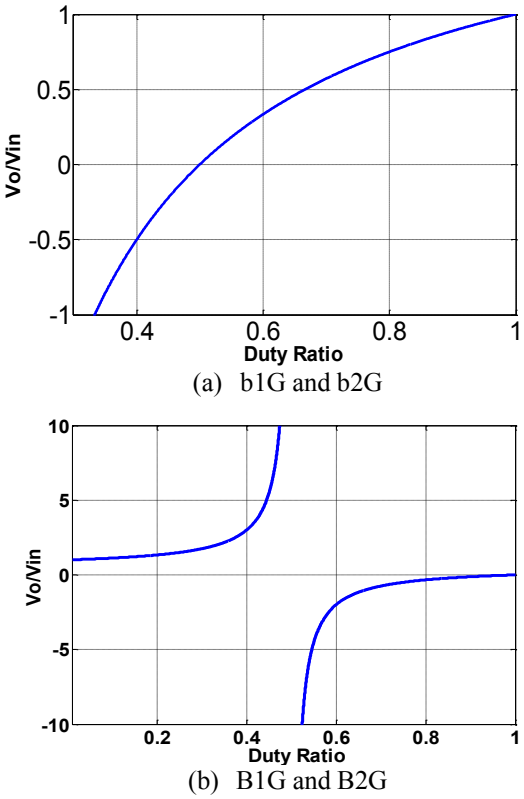
$$M(D) = \frac{1-D}{1-2D} \quad for \ \ B1G \ \ and \ \ B2G \tag{3}$$

Converter duty ratio D can be defined as:

$$D = t_{on} / t_s \tag{4}$$

where t_{on} is the duration when switch S_1 is on, and t_s is the total switching period.

Voltage conversion ratios (2) and (3) can be plotted against the duty ratio variation as shown in Fig. 3.



(a) b1G and b2G

(b) B1G and B2G

Fig. 3. Voltage conversion ratio M versus duty ratio D.

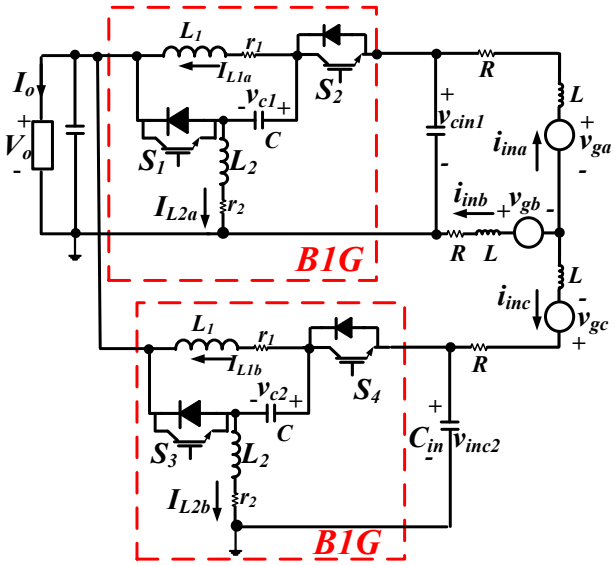
3 Four-Switch Three-Phase DC-AC Rectifiers

The converters shown in Fig. 2(c) and in Fig. 2(d) can both be configured for three-phase operation, as shown in

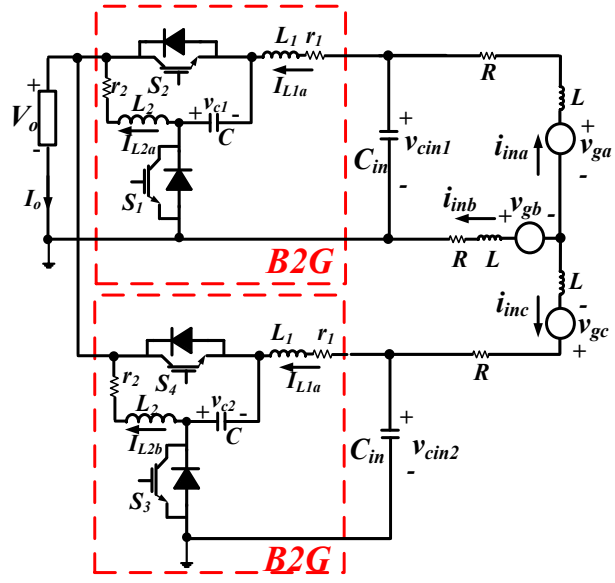
Fig. 4(a) and (b) respectively, resulting in four-switch three-phase rectifiers. Each boost converter represents one leg of the rectifier, whilst the third phase is connected to ground. The time-variant duty ratios, δ_1 and δ_2, are calculated from:

$$\delta_1(t) = \frac{V_o - v_{cin1}(t)}{2V_o - v_{cin1}(t)} \tag{5}$$

$$\delta_2(t) = \frac{V_o - v_{cin2}(t)}{2V_o - v_{cin2}(t)} \tag{6}$$



(a)



(b)

Fig. 4. Proposed FSTP rectifiers.

The output three-phase voltage can be expressed as:

$$\begin{aligned} v_{ga}(t) &= V_g \sin \omega t \\ v_{gb}(t) &= V_g \sin(\omega t - 2/3\,\pi) \\ v_{gc}(t) &= V_g \sin(\omega t + 2/3\,\pi) \end{aligned} \tag{7}$$

The generated voltages across capacitors v_{cin1} and v_{cin2} are:

$$\begin{aligned} v_{cin1}(t) &= V_m \sin(\omega t + \theta) \\ v_{cin2}(t) &= V_m \sin(\omega t + \theta + 1/3\,\pi) \end{aligned} \tag{8}$$

where $\omega = 2\pi f$ is the angular frequency. This causes three-phase currents i_{ina}, i_{inb} and i_{inc} to flow from the grid as follows:

$$\begin{aligned} i_{ina}(t) &= I_{in} \sin(\omega t + \gamma) \\ i_{inb}(t) &= I_{in} \sin(\omega t - 2/3\,\pi + \gamma) \\ i_{inc}(t) &= I_{in} \sin(\omega t + 2/3\,\pi + \gamma) \end{aligned} \tag{9}$$

where

$$\theta = \tan^{-1}\left\{\frac{\begin{array}{l}\omega L I_{in}\left(\sqrt{3}/2\,\sin(\gamma) - 3/2\,\cos(\gamma)\right) - \\ R I_{in}\left(3/2\,\sin(\gamma) + \sqrt{3}/2\,\cos(\gamma)\right) + \sqrt{3}/2\,V_g\end{array}}{\begin{array}{l} R I_{in}\left(\sqrt{3}/2\,\sin(\gamma) - 3/2\,\cos(\gamma)\right) + \\ \omega L I_{in}\left(3/2\,\sin(\gamma) + \sqrt{3}/2\,\cos(\gamma)\right) + 3/2\,V_g\end{array}}\right\} \tag{10}$$

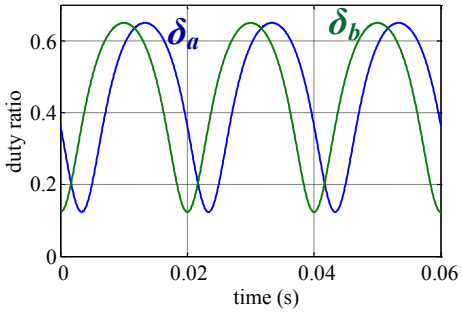
and

$$V_m = \frac{\begin{array}{l} R I_{in}\left(\sqrt{3}/2\,\sin(\gamma) - 3/2\,\cos(\gamma)\right) + \\ \omega L I_{in}\left(3/2\,\sin(\gamma) + \sqrt{3}/2\,\cos(\gamma)\right) + 3/2\,V_g\end{array}}{\cos(\theta)} \tag{11}$$

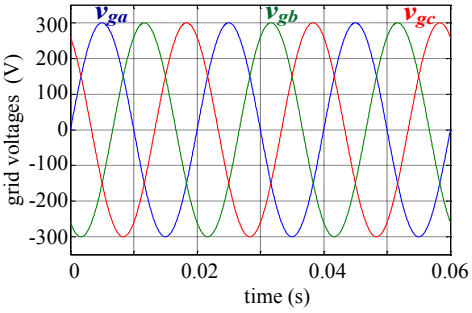
Parameter	Value
f	50 Hz
t_s	33 µs (switching period)
C_{in}	1 µF (Fig. 4(a)) and 5 µF (Fig. 4(b))
C_o	2000 µF
L_1, r_1	1 mH, 0.05 Ω
L_2, r_2	1 mH, 0.05 Ω
L	500 µH
R	0.5 Ω
V_g	300 V
V_o	600 V

Table 1: Parasitic Component Values and Circuit Conditions.

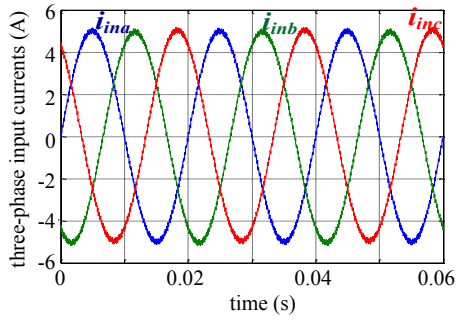
Fig. 5 and Fig. 6 show the open-loop operation of the rectifiers shown in Fig. 4 with the circuit conditions given in Table 1.



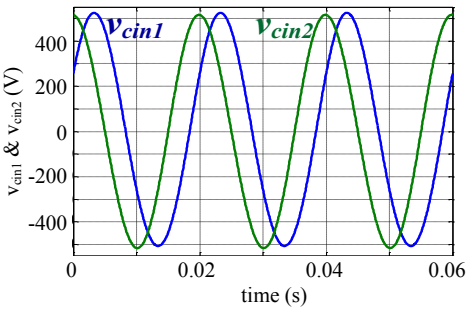
(a) Duty ratios δ_1 and δ_2



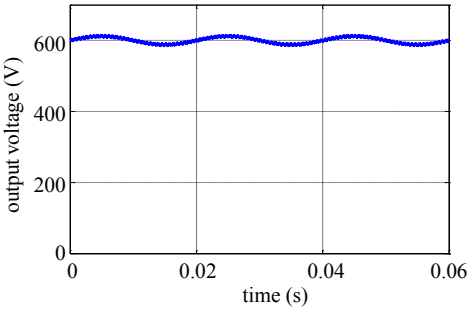
(b) grid three-phase voltage v_{ga}, v_{gb}, and v_{gc}



(c) grid three-phase current i_{ina}, i_{inb}, and i_{inc}

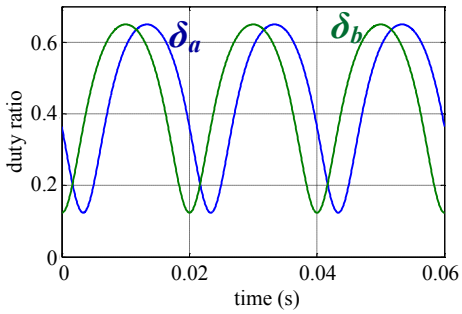


(d) Converters voltages v_{cin1} and v_{cin2}

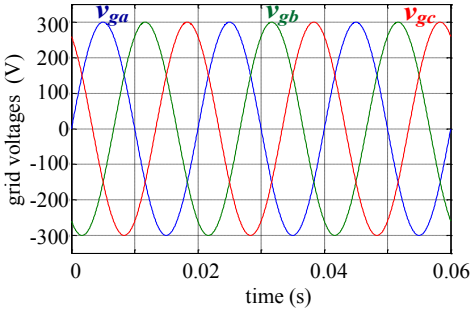


(e) output dc voltage

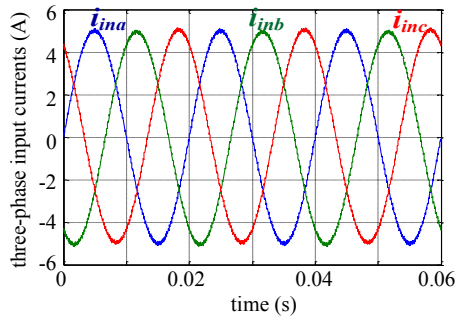
Fig. 5. Open-loop B1G rectifier operation.



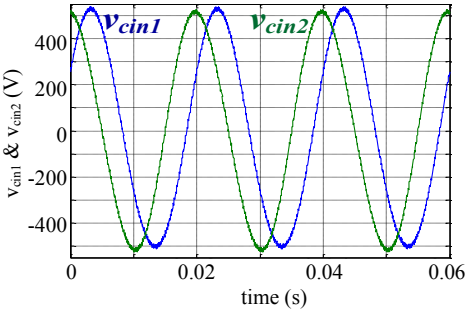
(a) Duty ratios δ_1 and δ_2



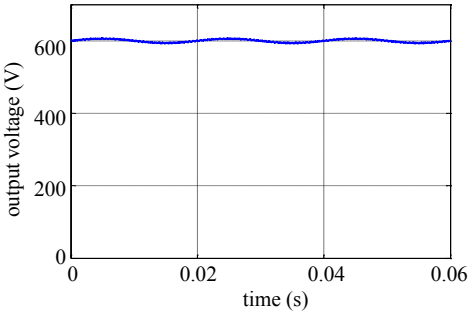
(b) grid three-phase voltage v_{ga}, v_{gb}, and v_{gc}



(c) grid three-phase current i_{ina}, i_{inb}, and i_{inc}



(d) Converters voltages v_{cin1} and v_{cin2}

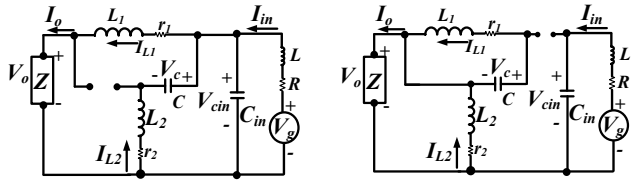


(e) output dc voltage

Fig. 6. Open-loop B2G rectifier operation.

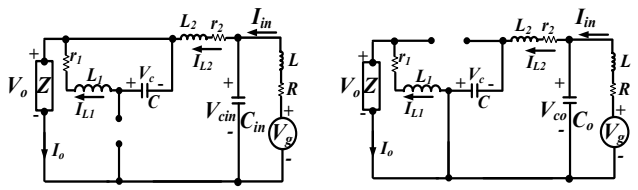
3 State-Space Modelling and Control Strategy

The B1G and B2G converter circuit configurations are shown in Fig. 7 and Fig. 8, which include the inductor parasitic resistances r_1 and r_2, and the output inductance and resistance L and R. The duration t_{on} defines the period that either S_1 or its anti-parallel diode is conducting. The average models of the converters are expressed in (12) and (13). The converter pole-zero maps in Fig. 9 and Fig. 10 show that the dynamics of the converters change with the small-signal duty ratio δ.



(a) $0 \le t < t_{on}$ (b) $t_{on} \le t < t_s$

Fig. 7. B1G converter configurations.



(a) $0 \le t < t_{on}$ (b) $t_{on} \le t < t_s$

Fig. 8. B2G converter configurations.

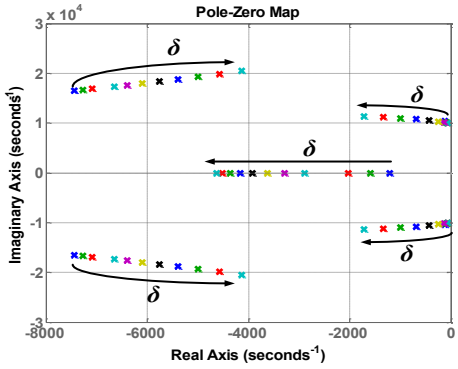


Fig. 9. B1G converter pole-zero map.

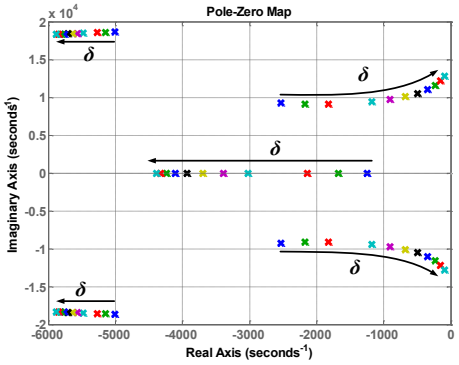


Fig.10. B2G converter pole-zero map.

$$\begin{bmatrix} \dot{I}_{L1} \\ \dot{V}_c \\ \dot{I}_{L2} \\ \dot{V}_{cin} \\ \dot{I}_{in} \end{bmatrix} = \begin{bmatrix} \frac{-r_1}{L_1} & \frac{1-D}{L_1} & 0 & \frac{-D}{L_1} & 0 \\ \frac{(-D)}{C} & 0 & \frac{-D}{C} & 0 & 0 \\ 0 & \frac{D}{L_2} & \frac{-r_2}{L_2} & \frac{-D}{L_2} & 0 \\ \frac{-D}{C_{in}} & 0 & \frac{D}{C_{in}} & 0 & \frac{1}{C_{in}} \\ 0 & 0 & 0 & \frac{-1}{L} & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} I_{L1} \\ V_c \\ I_{L2} \\ V_{cin} \\ I_{in} \end{bmatrix} + \begin{bmatrix} \frac{-D}{L_1} & 0 \\ 0 & 0 \\ \frac{D-1}{L_2} & 0 \\ 0 & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} V_o \\ V_g \end{bmatrix} \quad (12)$$

$$\begin{bmatrix} \dot{I}_{L1} \\ \dot{V}_c \\ \dot{I}_{L2} \\ \dot{V}_{cin} \\ \dot{I}_{in} \end{bmatrix} = \begin{bmatrix} \frac{-r_1}{L_1} & \frac{D}{L_1} & 0 & 0 & 0 \\ \frac{D}{C} & 0 & \frac{1-D}{C} & 0 & 0 \\ 0 & \frac{1-D}{L_2} & \frac{-r_2}{L_2} & \frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & \frac{-1}{C_o} \\ 0 & 0 & 0 & \frac{-1}{L} & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} I_{L1} \\ V_c \\ I_{L2} \\ V_{cin} \\ I_{in} \end{bmatrix} + \begin{bmatrix} \frac{D-1}{L_1} & 0 \\ 0 & 0 \\ \frac{-D}{L_2} & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L} \end{bmatrix} \begin{bmatrix} V_o \\ V_g \end{bmatrix} \quad (13)$$

Because the proposed inverters are high-order systems, Variable Structure Control [13] (VSR) is an attractive solution. Sliding Mode Control (SMC) [13], which belongs to a family of VSR techniques, is applied to the proposed rectifier. To shows the validity of the concept, the SMC for the proposed rectifier (B1G) is shown in Fig. 11, where r_1 and r_2 are the parasitic resistances of L_1 and L_2 respectively. K_1, K_2, K_3 are controller gains, which are selected as per [14]. Fig. 12 shows the experimental results for the B1G rectifier when load Z = 55Ω. The efficiency of the rectifier is 97%.

4 Conclusion

This paper presents new ac-dc rectifier topologies, based on bidirectional dc-dc converters, with reduced numbers of switches. The proposed rectifiers have better voltage utilisation than the conventional FSTP rectifier and do not draw dc currents from the input dc side. Single-phase rectifiers with fewer switches and better voltage utilisation factor can be obtained from the same power converters. State

space representation was used to demonstrate the dynamic response and robustness of the proposed rectifiers. However, the proposed inverters are high-order systems where the transfer function poles move with duty ratio variation. Consequently, classical control strategies are not easily implemented with these converters. The basic control structure, control design using sliding mode controllers, and MATLAB/SIMULINK results are presented, along with practical results to substantiate the design flexibility of the proposed topologies when controlled using a TMSF280335 DSP. Full comparisons between the proposed types of rectifiers, as well as conventional rectifiers in the literature, in terms of power loss, voltage regulation, THD, etc. will be considered in future publications.

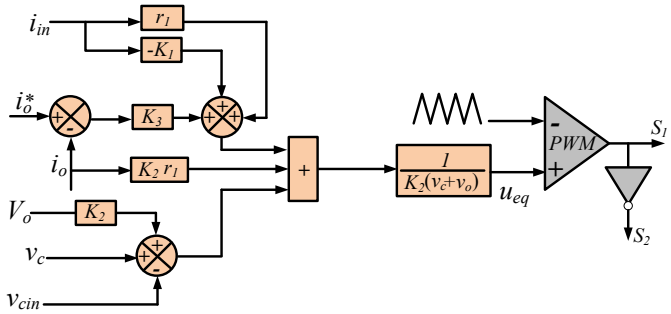
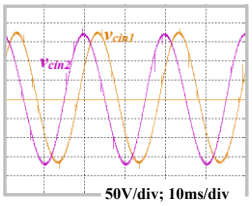
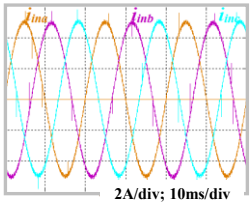


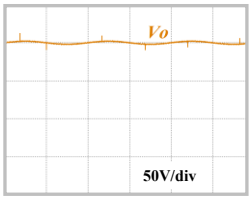
Fig. 11. FSTP rectifier sliding mode control.



(a) converter input voltages



(b) input current i_{ina}, i_{inb}, i_{inc}



(b) output dc voltage

Fig. 12. Experimental results for B1G FSTP (V_g = 100V, V_o = 200V and Z = 55 Ω).

Acknowledgement

The authors gratefully acknowledge the support of the EPSRC Underpinning Power Electronics 2012: Converters Theme project, Grant No. EP/K035096/1.

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